

REMARKS

Claims 1 - 31 were pending in the present application for patent as of the Office Action of March 11, 2005. In the Office Action of March 11, 2005, the Examiner objected to claims 5, 8, 9, and 28; rejected claim 25 under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention, rejected claims 26 and 27 under 35 U.S.C. 102(b) as being anticipated by US 5,301,084, Miller, rejected claims 1 - 5, 8, 14, 16, 17, 22 - 25, and 28 - 31 under 35 U.S.C. 103(a) as being unpatentable over Miller in view of US 6,385,021, Takeda et al and "Sub-Micron Chip ESD Protection Schemes Which Avoid Avalanching Junction", by Worley et al., rejected claims 6, 7, and 9 under 35 U.S.C. 103(a) as being unpatentable over Miller in view of Takeda et al, and Worley et al, and US 5,034,845, Murakami, and objected to claims 10, 15, and 18 as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 5, 8, 9, and 28 were objected to. In response, the applicants have amended claims 8 and 28 in a manner believed to overcome the objection. Regarding the objection of claims 5 and 9, the applicants believe the antecedent basis of the claimed "the second output" in dependent claims 5 and 9 is correct because "a second output" is claimed in claim 1, line 18. Therefore, the applicants respectfully request that the examiner withdraw the objection to claims 5, 8, 9, and 28.

Claim 25 was rejected under 35 U.S.C. 112, second paragraph. In response, the applicants have amended claim 25. The applicants believe that claim 25, as amended, is allowable under 35 U.S.C. 112, second paragraph.

Claims 26 and 27 were rejected under 35 U.S.C. 102(b) as being anticipated by Miller. The applicants have amended claim 26 to claim that the first bus is a positive power supply voltage bus and the second bus is a boosted voltage bus, where the boosted voltage bus is at a higher voltage than the positive power supply voltage bus. Also, claim 26 has been amended to claim that the detection circuit is coupled to a ground bus and to the internal node, and the pull-up circuit is coupled to the internal node, a boosted voltage bus, and a positive power supply voltage bus. FIG. 8 of Miller shows four power supply rings labeled "DVCC", "VCC",

"VSS", and "DVSS". However, Miller does not show or suggest a trigger circuit as claimed in amended claim 27, where, for example, an internal node of the trigger circuit is coupled to a positive power supply voltage bus during normal operation, and then to a boosted voltage bus during an ESD event. Also, Miller does not show or suggest a pull-up circuit coupled to an internal node, a boosted voltage bus, and a positive power supply voltage bus. Therefore, the applicants believe that claim 26, as amended, is allowable over Miller.

The applicants believe that the above comments regarding the rejection of claim 26 also apply to the rejection of amended claim 27, and that amended claim 27 is allowable over Miller.

Claims 1 - 5, 8, 14, 16, 17, 22 - 25, and 28 - 31 were rejected under 35 U.S.C. 103(a) as being unpatentable over Miller in view of Takeda et al and Worley et al. In accordance with the examiner's indication of allowable subject matter, the applicants have amended claim 1 to include the subject matter of claim 15. Claim 15 has been canceled. The applicants believe that claims 1 - 5, 8, 14, 16, 17, 22 - 25, as amended, are allowable over Miller in view of Takeda et al and Worley et al. Also, the applicants believe that claims 28 and 29 are allowable for at least the reasons given above for amended claim 26.

Claim 30 has been amended to claim that a boosted voltage bus provides a boosted voltage to first and second control terminals of a shunting circuit during an ESD event. Also, claim 30 has been amended to claim that a positive power supply voltage is provided to the first and second control terminals during normal operation, where the boosted voltage is higher than the positive power supply voltage. Claim 31 has been amended to claim that the shunting circuit comprises first and second cascoded transistors coupled between the ESD bus and the ground bus. Worley et al. discloses a shunting circuit with two control terminals. However, Worley et al. does not disclose one of the control terminals of the shunting circuit being supplied with a positive power supply voltage while the other terminal is at ground during normal operation. Therefore, the applicants believe that claims 30 and 31, as amended, are allowable over Miller in view of Takeda et al and Worley et al.

Claims 6, 7, and 9 were rejected under 35 U.S.C. 103(a) as being unpatentable over Miller in view of Takeda et al, and Worley et al, and Murakami. Claims 6, 9, 10, and 18 have been amended in order to conform claims 6, 9, 10, and 18 to amended claim 1. The applicants

believe that claims 6, 7, and 9 are allowable for at least the reasons given above for amended claim 1.

No amendment made was related to the statutory requirements of patentability unless expressly stated herein. No amendment made was for the purpose of narrowing the scope of any claim, unless the applicants have argued herein that such amendment was made to distinguish over a particular reference or combination of references.

Believing to have responded to each and every rejection contained in the Office Action mailed March 11, 2005, the applicants respectfully request the reconsideration and allowance of claims 1 - 14 and 16 - 31, as amended herein; thereby placing the application in condition for allowance.

Respectfully submitted,

SEND CORRESPONDENCE TO:

Freescale Semiconductor, Inc.
Law Department

Customer Number: 23125

By:



Daniel D. Hill

Attorney of Record

Reg. No.: 35,895

Telephone: (512) 996-6839

Fax No.: (512) 996-6854